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Himanshu S. Amin

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In re patent application of:

Applicant(s): Khoi A. Phan, et al.

Examiner: John S. Ruggles

Serial No: 10/050,417

Art Unit: 1756

Filing Date: January 16, 2002

Title: METHODS AND SYSTEMS FOR CONTROLLING RESIST RESIDUE
DEFECTS AT GATE LAYER IN A SEMICONDUCTOR DEVICE
MANUFACTURING PROCESS

Mail Stop After Final
Commissioner for Patents
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REPLY TO FINAL OFFICE ACTION DATED OCTOBER 23, 2003

Dear Sir:

Favorable reconsideration of the above-identified patent application is respectfully requested in view of the amendments and comments below.